Self-Limited Switching in Ta_2O_5/TaO_x Memristors Exhibiting Uniform Multilevel Changes in Resistance

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To facilitate the development of memristive devices, it is essential to resolve the problem of non-uniformity in switching, which is caused by the random nature of the filamentary switching mechanism in many resistance switching memories based on transition metal oxide. In addition, device parameters such as low- and high-state resistance should be regulated as desired. These issues can be overcome if memristive devices have switching limits for both the low- and high-resistance states and if their resistance values are highly controllable. In this study, a method termed self-limited switching for uniformly regulating the values of both the low- and high-resistance states is suggested, and the circuit configuration required for the self-limited switching is established in a Ta_2O_5/TaO_x memristive structure. A method of improving the uniformity of multi-level resistance states in this memristive system is also proposed.

1. Introduction

The memristor is one of the nanoelectronic devices that have been spotlighted in past decades[1–3] for their possible applications in passive circuit elements,[4–6] nonvolatile memory,[7–12] neuromorphic,[13–15] and reconfigurable logic devices.[16–18] Recently developed high performance memristor materials are accelerating the realization of these devices.[7–9,19] Meanwhile, in order to increase the use of memristor-based devices and to expand the number of applications in which they can be employed, the resistance of memristors should be uniformly controllable at desirable multiple levels. However, there is fundamental limit to achieve the uniform multiple resistance states in oxide-based memristor systems, where the rearrangement of the ionic defects is mostly responsible for the resistance switching (RS) phenomenon.[18–28] Because most of the oxide films contain various types of randomly distributed crystallographic defects and nonflat interfaces with the polycrystalline electrode, it is generally improbable to ensure the uniform defect arrangements in all the memristor cells. Although several reports on the uniform multilevel switching have been made,[29–34] this intrinsic uncertain and uncontrollable nature of RS behavior still remains unsolved. Nevertheless, switching uniformity can be ensured by configuring an appropriate peripheral circuit with the memristive element as shown in this report. The nonuniformity has been induced during both set (switching from high-resistance state (HRS) to low-resistance state (LRS)) and reset (LRS → HRS) switching. It is well known that limiting the maximum current (compliance current) during the set switching is effective in forming a uniform LRS resistance (R_{LRS}) and in protecting the device from permanent electrical damage.[35–39] Moreover, by adjusting the maximum current level, multiple resistance states can be attained. However, actual device can hardly incorporate such complicated circuitry due to economical reasons. Therefore, achieving multilevel resistance values during the set switching is generally very challenging. Meanwhile, few studies have investigated methods of controlling the resistance of HRS (R_{HRS}) during reset switching. In order to use the memristor as the analog circuit device or the multilevel information storage, however, the control of the reset switching is also important to attain the wider range of intermediate states. In addition, the reset switching could show a gradual resistance change behavior compared with the rapid resistance change during the set switching, and, thus, control the reset switching could be a viable method to achieve the uniform multilevel switching.[29–34]

In this study, therefore, a method of implementing "self-limited" reset switching is suggested and demonstrated. Then it is realized via a Ta_2O_5/TaO_x ($x \approx 2$) structure. Using this method, both set and reset switching could be well regulated, which would allow self-limited R_{LRS} and R_{HRS} values. Here, the term "self-limited" refers to the circumstance where the R_{LRS} and R_{HRS} values were saturated at a certain value even when the degree of electrical stimulus varied. The circuit model for implementing self-limited switching was presented and the experimental results from the Ta_2O_5/TaO_x memristor structure were precisely fitted according to the circuit model. Finally, uniform and precise multilevel programming using self-limited switching was presented.

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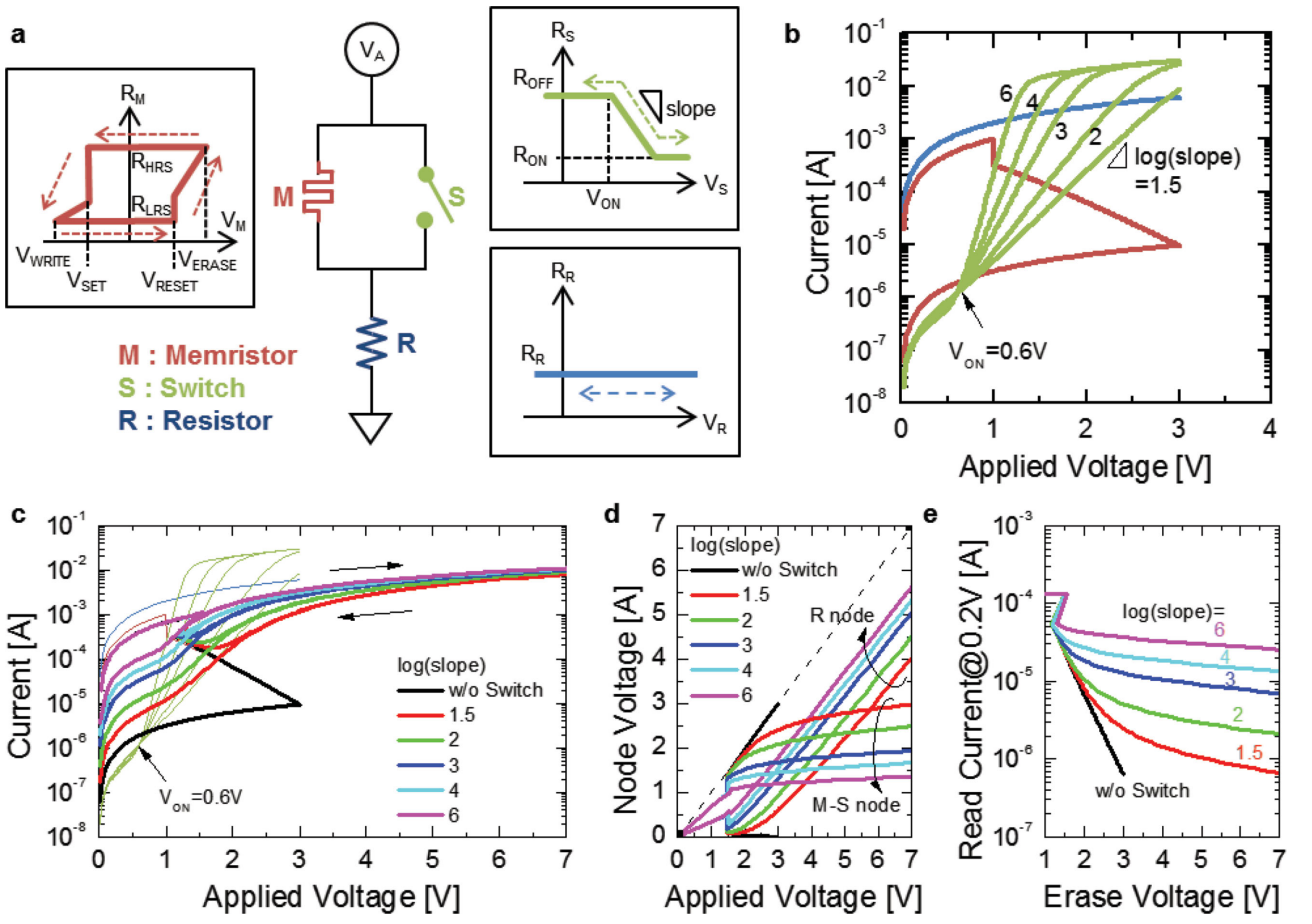

Figure 1. A self-limited switching circuit. a) Configuration of a self-limited switching circuit, composed of a bipolar memristor (M), a switch (S), and a resistor (R). The typical resistance–voltage characteristics of the M, S, and R are displayed. b) Sample *I*–*V* characteristics of M, S, and R for demonstration. For the simulation, the following values were used: R_R = 500 Ω, R_{OFF} = 10^6 Ω, R_{ON} = 100 Ω, V_{ON} = 0.6 V, log(slope) = 1.5–6 A decades V^{-1}, R_{LRS} = 10^3 Ω, R_{HRS} = $10^{5.5}$ Ω, V_{SET} = −1 V, and V_{RESET} = 1 V. c) Demonstrated *I*–*V* characteristics of the circuit. d) The node voltages depending on the applied voltage. e) Readout current at 0.2 V depending on the erase voltage (V_{ERASE}). When the S existed, the readout current was saturated despite the increase in the V_{ERASE}.

2. A Self-Limited Switching Model

Figure 1a shows the circuit configuration for the self-limited switching where three components, a resistor (R), a switch (S), and a bipolar RS (BRS)-type memristor (M), constitute the circuit. Here, S can be any switch, such as a threshold switch or a highly nonlinear insulator, as long as it shows abrupt enough current increase at a certain voltage. Due to the presence of the R in series with the M–S parallel circuit components, the set switching, thus, R_{LRS}, can be well regulated, which is already well-known in the field. The characteristic feature of this circuit configuration is the presence of S parallel to M, which regulates well the reset switching, thus, R_{HRS}. The typical resistance–voltage characteristics of the M, S, and R are also schematically displayed in Figure 1a. (The details of M, S, and R of this simulation are discussed in Section I, Supporting Information.) When these components with the appropriate resistance values (R_R of R, R_{ON} and R_{OFF} of S, R_{LRS}, and R_{HRS} of M), transition parameter values (V_{ON} and slope of S, and V_{SET} and V_{RESET} of M) were connected as shown in Figure 1a, the reset switching of the M could be precisely controlled by adjusting the value of slope and V_{ON}. Meanings of acronyms can be found from Figure 1a. Figure 1b shows an example of the *I*–*V* characteristics of the circuit elements at a semilogarithmic scale with various slope values for simulation. In this figure, a V_{ON} of 0.6 V was assumed. Figure 1c shows the simulated *I*–*V* characteristics of this circuit with various slope values. (The details of this simulation are discussed in Section I, Supporting Information.) Here, the bias voltage is applied over the entire circuit shown in Figure 1a, where M is initially in its LRS. Figure 1d shows the node voltage over the R (node R) and the parallel M and S (node M–S) in accordance with the slope of S. When the applied voltage reached 1.5 V, a reset switching of M was shown when the voltage over the M–S node reached V_{RESET} = 1.0 V of M where S still has the higher resistance value. Then most of the applied voltage is applied on the M–S node due to its higher resistance than R_R. As the applied voltage increased further, the conductance of S drastically increased and the total resistance of the M–S node decreased accordingly. Then, as shown in Figure 1d, the node voltage applied on the node R increased

while that of M–S node was saturated even though the increase of applied voltage. Such an operation of the circuit suggests that the voltage over the M element in the circuit could be retained well at a certain level even if the applied voltage increases to a very high level. This can eliminate the concerns with over-resetting and R_{HRS} fluctuation due to excessive voltage application or current flow through the M element. Figure 1e shows the simulated variations in the current measured at 0.2 V (read current) after the reset occurred as a function of the maximum applied voltage (V_{ERASE}) for various slope values. Even though the V_{ERASE} varied in a relatively large range, the read current, thus, the R_{HRS} value remained at a specific level, which was determined by slope value. This is the salient feature of this self-regulating circuit. In contrast, the read current varies largely when there is no switch in the circuit (black line) when the V_{ERASE} varies.

3. Self-Limited Switching Demonstration

To confirm the self-limited operation even more evidently, the self-limited circuit of Figure 1a was configured by using individual M, S, and R. For this experiment, the sputter-deposited 20-nm-thick single Ta_2O_{5-x} film as the RS layer was formed on the Pt bottom electrode (BE). Then, Ta top electrode (TE) was formed by the electron-beam evaporation method through a metal shadow mask with a hole diameter of 100 μm. The sputtering condition was carefully tuned to make the pristine single Ta_2O_{5-x} layer insulating enough not to arrow additional leakage current path except the localized conducting filaments (CF) after the electroforming. The thick thickness (20 nm) of the Ta_2O_{5-x} film also contributed to the low current. In other words, there should not be embedded S component in parallel configuration with the CFs after the electroforming, of which case will be discussed in the next section. **Figure 2**a shows the pristine *I–V* curves and subsequent RS curves of the $Ta/Ta_2O_{5-x}/Pt$ device. For this measurement, the BE Pt was biased while the TE Ta was grounded to make the switching directionality identical to that of the simulation. It can be understood that the pristine film has very insulating properties under both bias polarities. Therefore, this sample can safely represent only M component owing to the formation of the CFs after the electroforming. This device has a multilevel switching capability depending on the level of V_{ERASE}. Figure 2b shows enlarged *I–V* curves of Figure 2a which clearly shows the multilevel switching characteristics of this film. Among these curves, the switching curves of V_{ERASE} = 2.0 V was used for the following simulation, of which reason will be

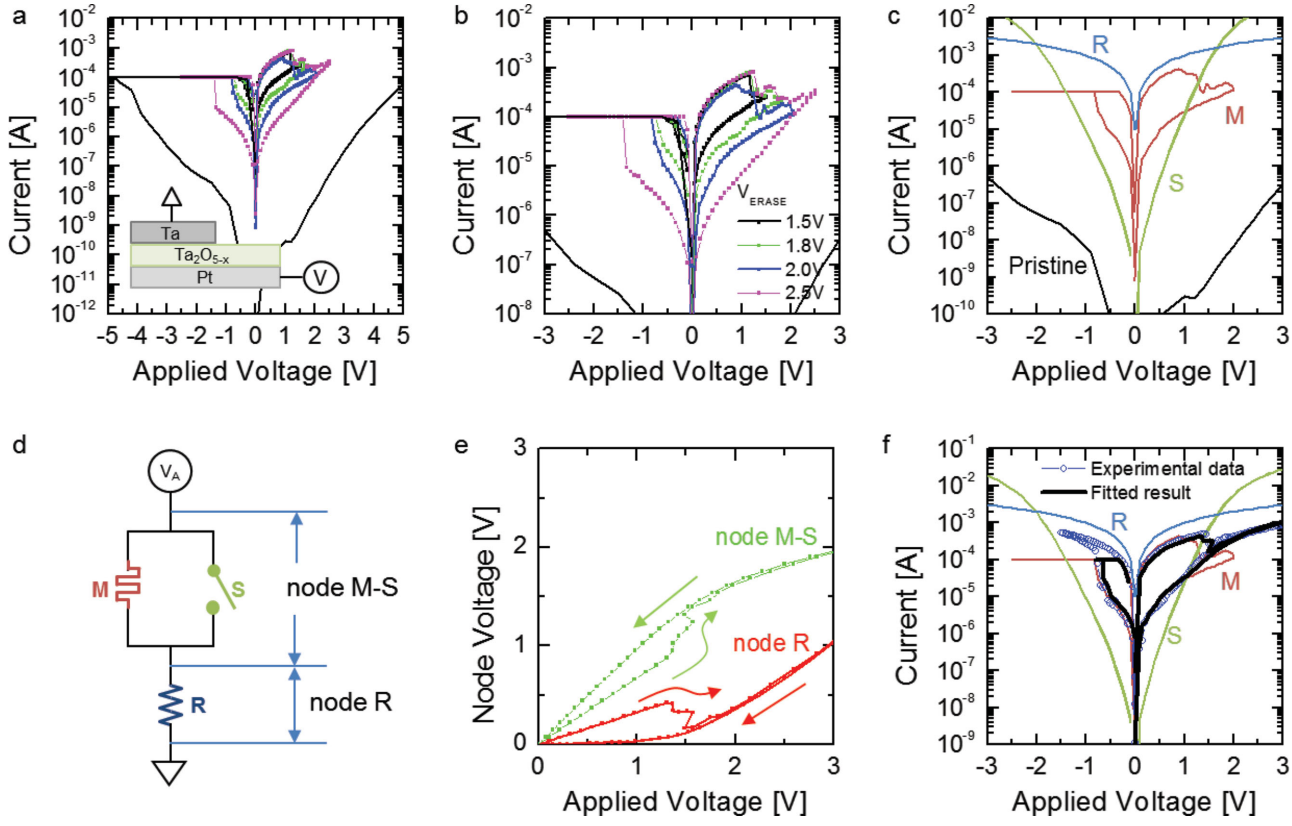

Figure 2. Externally configured self-limited switching experiment. a) The pristine *I–V* curves and subsequent resistance switching curves of the $Ta/Ta_2O_{5-x}/Pt$ device. The inset shows the device structure. b) Enlarged RS curves of a) depending on the V_{ERASE} to show the multilevel switching capability. c) The *I–V* characteristics of the individual R, M, and S. The pristine *I–V* of the $Ta/Ta_2O_{5-x}/Pt$ device is also included for comparison. d) Schematic diagram of the self-limited switching configuration. e) Calculated node voltage as a function of the applied voltage. f) The RS curves of the experimental data obtained from the self-limited configuration (blue dotted-line) and the simulated curves (black line).

explained. For the S, a TaN/Ta_2O_5/TaN stack was fabricated by the atomic layer deposition process. Here, the S stack was sandwiched by evaporated Pt layers to supplement the electrical conduction. Figure 2c shows the *I–V* characteristics of this stack (green line), which proves the highly nonlinear *I–V* property (high slope) of this material stack. For the R, 1k Ω of stand-alone resistor was used, of which *I–V* curve is also included in Figure 2c (blue line). Then, these devices are connected according to the circuit diagram shown in Figure 2d. Figure 2e shows the node voltage of this configuration, which is calculated as a function of the externally applied voltage according to Kirchhoff's law. Due to the voltage drop over R, the M–S node voltage was limited to 2 V for the 3 V of applied voltage which corresponds to the V_{ERASE}, while the node voltages show hysteretic behavior due to the switching of M. Therefore, the *I–V* of M with V_{ERASE} = 2.0 V in Figure 2b was selected for the circuit simulation. Figure 2f shows the *I–V* curves of the experiment (blue dotted line) and the simulation (black line) from the composed circuit. For this simulation, the experimental *I–V* curves of individual M, S, and R of Figure 2c were used. It is evident that they completely overlap each other suggesting that the circuit model adopted in this work is accurate. The only difference between the experiment and the simulation is the method limiting the current during the set switching. The compliance current of the simulation is associated with the adoption of the compliance current of the set switching of M, which was unnecessary for the composed circuit due to the presence of R.

4. Self-Limited Switching Realization Via a Ta_2O_5/TaO_x Memristor System

The circuit configuration shown in Figure 1a could be implemented into a memristor cell via a Ta_2O_5/TaO_x double layer structure. For this cell fabrication, a 20 nm-thick TaO_x was first sputter-deposited as shown in **Figure 3**a, which is named as R_i. The R_i will be divided into R and highly nonlinear insulator type of S by the followed oxidation process. Then, Ta_2O_5 layers were formed via cyclic plasma-oxidation of a part of TaO_x layer as shown in Figure 3b. (See the Experimental Section for details.) The amorphous Ta_2O_5 layer showed highly nonlinear *I–V* characteristics under the positive bias voltages where no electroforming could be induced.[40] This highly nonlinear *I–V* characteristics of Ta_2O_5 layer could be regarded as the S thus the *I–V* characteristics of R–S series configuration could be achieved from the *I–V* characteristics under the positive bias of the pristine sample. Then, the electroforming was performed by applying −3.5 V of negative bias on Ta_2O_5/TaO_x structure to form the CFs corresponding to the M as shown in Figure 3c. Park et al. confirmed the presence of ≈1–2 nm-diameter CFs, which is mainly comprised of TaO_{1-x} phase, in this structure by the in situ scanning transmission electron microscope (STEM) experiment.[41] Meanwhile, the area outside the CF region, called OCF, acts as the S which exists in parallel with the M. This OCF region has been generally considered inactive during the RS, despite its larger contact area than CF. However, this OCF is now regarded as the S, so that the self-limiting circuit

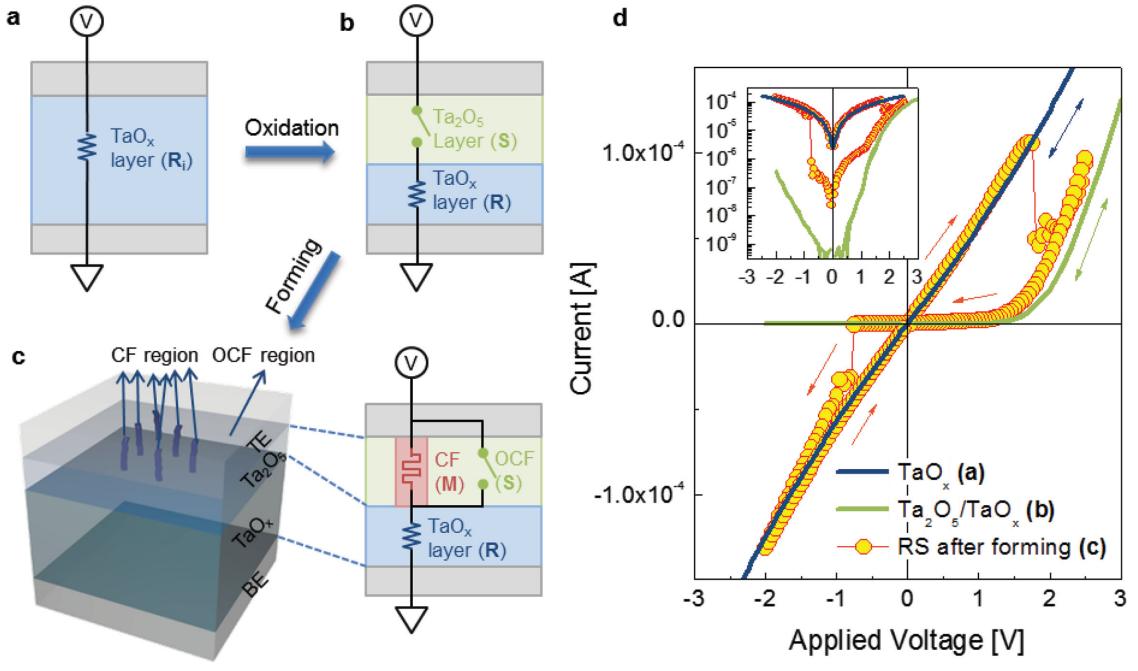

Figure 3. Experimental setup for self-limited switching via a Ta_2O_5/TaO_x system. Schematic representation of a) single layer TaO_x layer, which represent R_i, and b) bilayered Ta_2O_5/TaO_x structure, which can represent the series connection of R and S (R–S) under the positive bias region. c) shows the schematic representation (left panel) and the equivalent circuit (right panel). The localized conducting filament (CF) region and the area outside the CF region (i.e., the OCF region) are shown within the Ta_2O_5 layer. d) Typical bipolar resistance switching *I–V* curve of the Ta_2O_5/TaO_x sample after the electroforming (yellow symbols). It also shows the experimental *I–V* curves of R (single layer TaO_x, black line), and R–S (bilayered Ta_2O_5/TaO_x structure before electroforming, green line).

configuration in Figure 1 could be experimentally achieved after the electroforming under the negative bias. There must be sufficient area for S even for the sub-10 nm device considering the extremely small CF diameter. (More experimental evidence for the conduction through the OCF in HRS can be found in Section II, Supporting Information.) Figure 3d shows typical direct current (DC) *I–V* curves of the stacks in Figure 3a–c at the linear *I–V* scale (and the inset at the semilog scale) from a 1 μm × 1 μm area memory cell. Here, the *I–V* characteristics of TaO_x layer (R_i) and pristine Ta_2O_5/TaO_x layer (R–S in series) are closely related with the LRS and HRS of the RS sample after the electroforming. It is noticeable that *I–V* curves of the R_i and the LRS of RS sample (which corresponds to the series of R and M) overlap despite the much smaller area of CF. This is very reasonable considering the higher oxygen vacancy concentration and short length (and consequently the higher conductivity) of the CFs.[41] The actual R of the Ta_2O_5/TaO_x layer might be more conductive than R_i since a small portion of initial TaO_x layer was transformed to Ta_2O_5. In addition, a slightly higher current of HRS than the pristine sample in the high voltage region can be originated from the formation of the CF region. In this Ta_2O_5/TaO_x structure, both S and M can be regulated thus R_{HRS} can be precisely controlled as shown later.

The characteristics of S can be modulated by changing the thickness of the Ta_2O_5 layer in the device fabrication process, whereas the characteristics of M are insensitive to the thickness of the Ta_2O_5 layer because the actual RS occurs only in a certain portion of CF nearby the Pt electrode.[7] Three different devices (PO-40, PO-60, and PO-100, which were plasma-oxidized for 40, 60, and 100 cycles, respectively) were fabricated from the TaO_x layer (2.7% O_2 during the sputtering) and their RS behavior was examined. The Ta_2O_5 layers of the PO-40, PO-60, and PO-100 devices were approximately 6.2, 8.5, and 9.4 nm-thick, respectively. (See Section III, Supporting Information.) **Figure 4**a shows the DC *I–V* switching curves of the three devices at the semilogarithmic scale for the same V_{WRITE} (−2 V) and V_{ERASE} (+2.5 V) values. It was found that all the devices showed identical LRSs irrespective of their Ta_2O_5 thickness. This can be taken to mean that the LRS is the serial connection of TaO_x layer and CFs where the total length of conduction path is almost independent of the Ta_2O_5 thickness. However, as the number of oxidation cycles increased, the HRS current decreased for the same V_{ERASE} value. To ensure self-limited reset switching, the reset switching curves in Figure 4a (in the positive bias region) were deconvoluted, assuming that the memory cell was composed of R, S, and M. Figure 4b shows the deconvoluted *I–V* curves of R, S, and M from the experimental reset data in the positive bias region of Figure 4a (experimental data are represented by lines for comparison). For this deconvolution, the *I–V* curves of individual R, S, and M must be known, and *I–V* curves of R and S could be inferred from the experiment as aforementioned in Figure 3. The inset of Figure 4b shows the *I–V* curves of R (blue square symbol) and S (green square symbol) calculated accordingly.

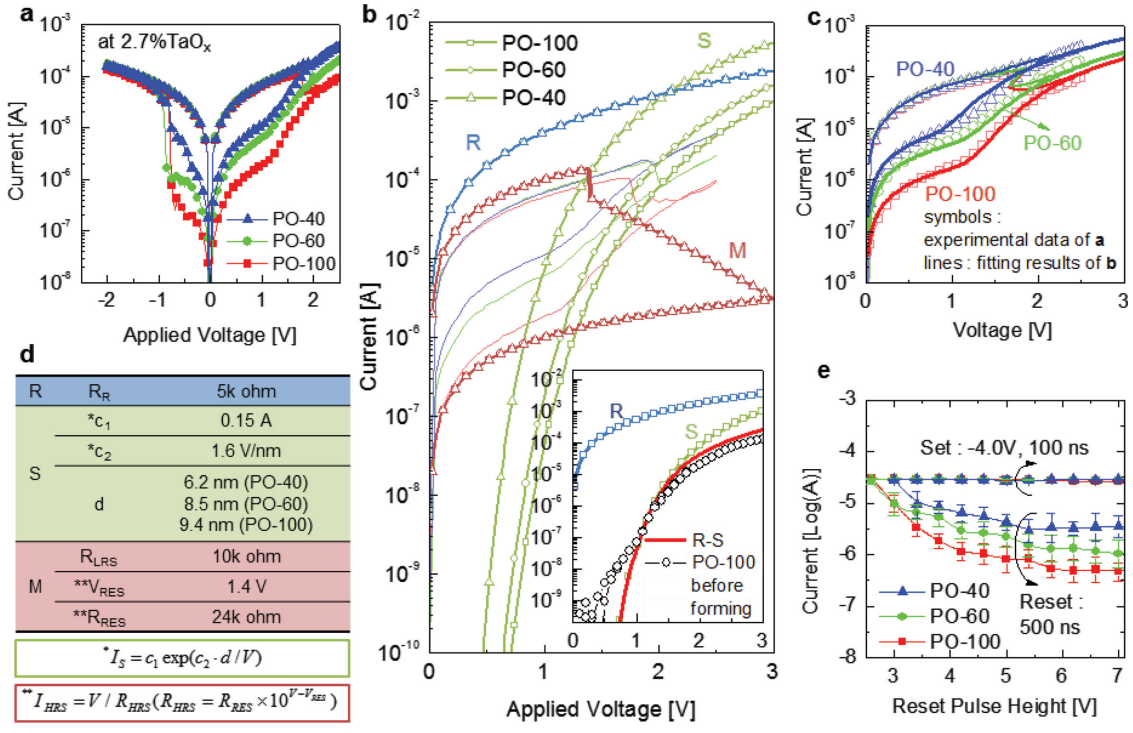

Figure 4. S modulation in self-limited switching in the bilayered Ta_2O_5/TaO_x structure. a) Resistance switching characteristics of the PO-40, PO-60, and PO-100 devices. b) Deconvoluted *I–V* curves of M, S, and R from the reset curves of (a). The inset shows good match between the expected *I–V* curve of R–S series connection (red line) from R and S of PO-100 and the experimental *I–V* curve of the pristine Ta_2O_5/TaO_x layer (open symbol). c) Experimental reset data and fitting results of the self-limited switching using the *I–V* characteristics of (b). d) Fitting parameters used for the deconvolution of (b). e) Pulse switching characteristics of these devices, which were dependent on the magnitude of the reset pulse. The magnitude of the set pulse was −4.0 V. The widths of the set and reset pulses were 100 and 500 ns, respectively.

The I–V curve of S could be physically modeled from the trap-assisted tunneling (TAT) of carriers through the thin Ta_2O_5 layer.[7,42] (See Section IV, Supporting Information, for details.) The black square symbol in the same inset figure showed the experimental I–V curve of the pristine Ta_2O_5/TaO_x layer, where the data of PO-100 were adopted. The red line corresponds to the calculated I–V curve of the series connection of R and S, showing the great match with the experimental data. The mismatch in low voltage region is due to the emergence of different conduction mechanism in that region, but this region is not relevant with the self-limited RS so it can be disregarded. I–V curves of S of other samples could be similarly determined (green symbols in Figure 4b). Then, the I–V of M can be calculated as represented by the red symbols in Figure 4b. It is notable that only S varies according to the thickness of the Ta_2O_5 layer. Figure 4c shows the fitted reset switching curves (lines) with the experimental reset switching data reproduced from Figure 4a (open symbols). The excellent match between the experimental and simulation results confirms the validity of the circuit model adopted to explain the DC I–V switching curves. Figure 4d shows the summary of the parameters used for the deconvolution. The key ingredient of this simulation is that the HRS of the M can be precisely adjusted by changing the characteristics of the S, which are determined in the oxidation process. Such a novel operation of the RS memory can be further confirmed by the pulse switching results shown in Figure 4e. In this case, the set was achieved by applying a short pulse of −4 V in amplitude and a 100 ns duration, and the reset was achieved by applying a longer pulse of 500 ns with different amplitudes of 2.5–7.0 V. The constant set state current measured at 0.2 V (thus, R_{LRS}), irrespective of the Ta_2O_5 thickness, was reconfirmed. More importantly, the reset state current measured at the same voltage (thus, R_{HRS}) values were saturated to a certain value when the reset pulse height was > ≈5.5 V, and the saturation level was determined by the Ta_2O_5 thickness. This means the functionality of S can be adjusted by varying the thickness of the Ta_2O_5 layer, whereas those of M and of R are not influenced by it, and these results coincide very well with the circuit modeling shown in Figure 1.

The characteristics of the M can also be regulated by modulating the CF region. This can be achieved by changing the compliance current (I_{CC}) during the DC I–V sweep or the set pulse voltage in the pulse switching. For this experiment, a sample with TaO_x layer deposited under the oxygen concentration of 2.5% followed by 60 cycles-plasma-oxidized Ta_2O_5 layer was selected. The slightly lower oxygen concentration resulted in slightly lower resistance of the TaO_x layer. These R and S combinations provided appropriate R_R, V_{ON}, and slope values to ensure the regulation characteristic of the M. **Figure 5**a shows the RS curves obtained by controlling I_{CC} (to 60–100 μA) during the set switching. As the CF became stronger (i.e., as the corresponding R_{LRS} value decreased), the V_{RESET} value increased and the HRS current increased for the given V_{ERASE} value (2.5 V). The experimental reset I–V curves in Figure 5a are deconvoluted (Figure 5b), using a constant experimental

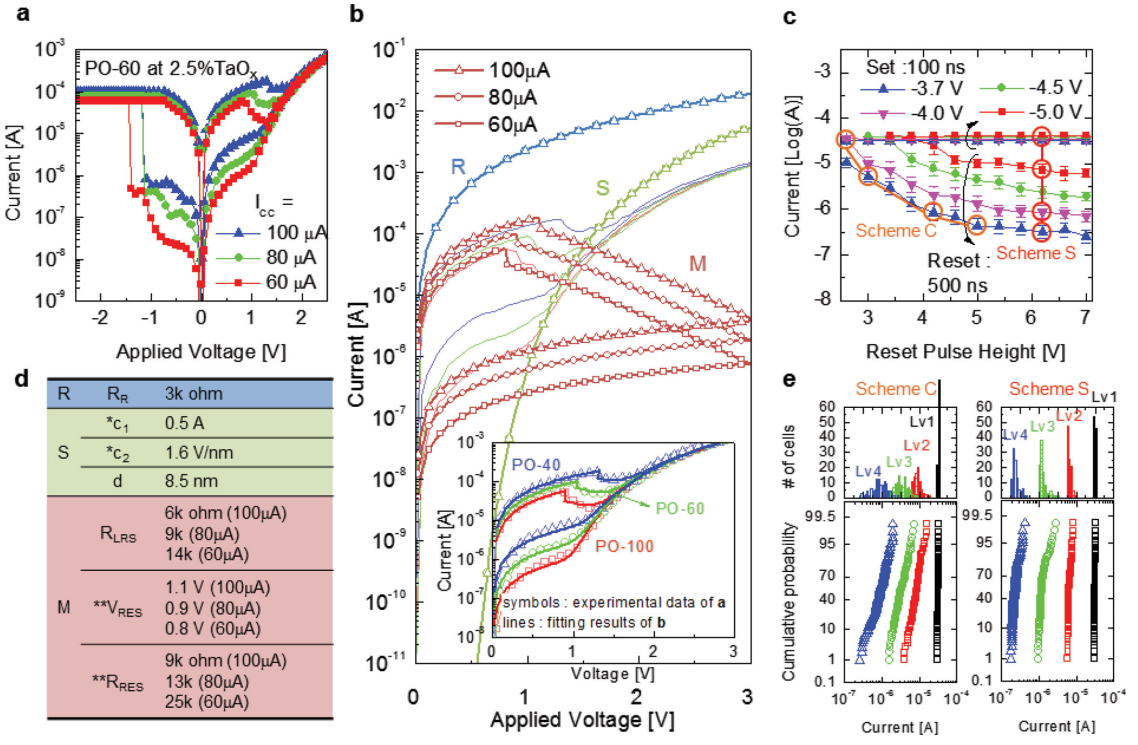

Figure 5. M modulation in self-limited switching in the bilayered Ta_2O_5/TaO_x structure. a) Resistance switching characteristics of 2.5%-PO-60 depending on the compliance current. b) Deconvoluted I–V curves of M, S, and R from the reset curves of (a). The inset shows the experimental reset data and fitting results. c) Pulse switching characteristics of these devices. The widths of the set and reset pulses were 100 and 500 ns, respectively. d) Fitting parameters used for the deconvolution of (b). e) Improvement in the uniformity of multilevel switching due to self-limited switching. Left panel shows the multilevel switching uniformity of Scheme C and right panel shows that of Scheme S. Each operation schemes are indicated by large circles in (c).

R value (the blue symbol), which is ascribed to the TaO_x layer, and a single curve of S (the green symbol), which is consistent with what was used in Figure 4b, as well as different M functions, as represented by the brown symbols in Figure 5b. The inset of Figure 5b shows the fitting results using these R, S, and M functions to the experimental data, and Figure 5d shows the fitting parameters. Fitting results are also excellent, suggesting the accuracy of the circuit model. From these results, it is clear that the varying I_{CC} values changed only the status of CF, whereas the others (the TaO_x layer and the OCF region) were hardly influenced by the different I_{CC} values. The pulse switching results summarized in Figure 5c also confirm the usefulness of such operation. In this case, the functionality of different I_{CC} values in the DC *I–V* sweep was emulated by adopting different set pulse voltages while keeping the set pulse duration constant (100 ns). The current at 0.2 V for the LRS was again confirmed to have increased with the absolute set pulse height. The current at 0.2 V for the HRS increased with the increasing absolute set pulse height but was saturated at a certain level, which is determined by the previous set pulse height, even when the reset pulse height increased. These results prove that the M is successfully regulated without inducing any change in the R and the S.

This characteristic can be used for self-limited "multilevel" switching. Self-limited multilevel switching means that not only the LRS and HRS but also the multiple intermediate states between them can be defined in a self-limited manner. When enough levels have been uniformly programmed, increase in the memory data density and even the analog memristor could be achieved. Figure 5e shows the uniformity of the multilevel switching by the conventional operation scheme (Scheme C, left panel) and by the self-limited operation scheme (Scheme S, right panel). In the Scheme C, the reset pulse height was varied from 3.0 to 5.0 V for the given set pulse height of −3.7 V to change the R_{HRS}. These reset pulse height range corresponds to ≈1–1.7 V range in DC *I–V* curves of I_{CC} = 80 μA sample in Figure 5b, where the S is still remained off thereby the self-limited mechanism hardly works. In this scheme, the high resistance levels showed significant fluctuations, and thus, could not be distinguished easily. In the Scheme S, however, the set pulse height was varied to −3.7, −4.5, or −5.0 V to control the strength of the CF for the given reset pulse height of 6.2 V, which corresponds to ≈2 V in DC *I–V* of Figure 5b, thereby the self-limited mechanism works. Although the differences between these LRSs were not large as can be seen in Figure 5c, so they should be regarded as level 1, their reset switching behaviors are very distinguishable as shown in Figure 5b. Therefore, the followed reset switching amplified the subtle differences between the LRSs thus the clearly distinguishable HRS levels (levels 2, 3, and 4) could be achieved. It is very important to note significant improvements in the uniformities of the HRS levels could be achieved by adopting this scheme. This phenomenon can be understood on the basis of the distributions of the resistance values. The distribution in the Scheme C (top-left panel in Figure 5e) has a normal Gaussian form, whereas that in the Scheme S was skewed (top-right panel in Figure 5e). This was because in the latter case, the turned on S drained off the excessive current, which eliminated the over-reset during the self-limited reset switching.

5. Conclusion

In conclusion, a RS memory cell with self-limited switching configuration composed of the memristor, switch, and resistor to limit both the set and reset switching in a self-regulating manner was proposed and realized using a Ta_2O_5/TaO_x structure. Due to the switch-like highly nonlinear behavior of the OCF region in the Ta_2O_5 layer, which was parallel to the memristor, the over-resetting or nonuniform resetting effects were sufficiently suppressed and a highly uniform reset state was achieved. The series resistor enhanced the set state uniformity and helped to enhance the reset state uniformity. In the experiment, the switch and memristor characteristics were regulated by modulating the thickness of Ta_2O_5 layer and by changing the compliance current (or the set pulse voltage height) during the set switching, respectively. The series resistance was easily adjusted by changing the oxygen concentration in the TaO_x base layer. These regulation methods showed that self-limited switching can facilitate uniform switching even with multilevel resistance values. In particular, the memristor modulation method can successfully achieve multilevel switching that involves four levels due to the exploitation of the self-limited switching. Even from the same RS material system, the conventional programming scheme resulted in high nonuniformity of the different reset states, which made multilevel switching impractical.

6. Experimental Section

Preparation of the Ta_2O_5/TaO_x Devices: All the fabricated devices had a 1 μm × 1 μm crossbar array structure. A 50 nm-thick W layer was deposited on a 3 nm-thick adhesion Ti/500 nm-thick SiO_2/Si substrate via sputtering and then patterned via dry-etching to form the bottom electrode. Then a conducting 20 nm-thick TaO_x ($x \approx 2$) layer was deposited on the BE via DC magnetron sputtering in a reactive O_2 and Ar ambient with varying oxygen concentrations in the sputtering gas (2.5% and 2.7%) using a Ta target. Next, an insulating layer of Ta_2O_5 was formed via the pulsed O_2-plasma oxidation process. Each cycle of this oxidation process had the following two steps: a 2 s exposure to the plasma and a 4 s period with the plasma turned off. The total oxidation time was controlled by the number of cycles. For comparison, four devices were prepared via the plasma oxidation process, using 60 cycles for TaO_x with 2.5% oxygen concentration (2.5%-PO-60) and using 40 (PO-40), 60 (PO-60), and 100 cycles (PO-100) for TaO_x with 2.7% oxygen concentration, respectively. Finally, a 20 nm-thick Pt layer was deposited via electron-beam evaporation and patterned via the lift-off method. The fabrication process of test sample composed of single layer Ta_2O_{5-x} was described in Section 3.

Electrical Measurements: The DC-based electrical characterizations were performed using an Agilent 4156C semiconductor parameter analyzer (SPA) in the voltage-sweep mode. The pulse measurements were performed using an Agilent 81110A pulse generator. After the pulse application, the memory state was checked using the Agilent 4156C SPA. During the electrical measurement, the Pt top electrode was biased while the W bottom electrode was grounded.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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